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DESIGN AND APPLICATION OF ELECTRONIC HARDWARE BASED ON FPGA

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Abstract: Based on the traditional FPGA hardware structure, the paper proposed a new design and application suited to hardware system. Through the analysis of structure and principle of FPGA, a hardware design scheme combined FPGA and Matlab was completed. And the results of simulation testing of FPGA filter suggested that this system had less error and stronger ability of denoising, compared with the traditional FPGA.

Keywords: FPGA; Principle; System Structure; Simulation

1. Introduction

In the 21st century, the rapid development of information industry leads us into an information-based society comprehensively. The broad use of information technology in daily life deeply transfers people's traditional life style. As one of the pillars of the economy, information industry plays a key role in safeguarding state security and improving comprehensive national power [1-3]. And the integrated circuit becomes an important symbol to measure the scientific and technological progress and comprehensive national power of a country. We should strive to develop the industry of integrated circuit, to intensively study the design and technology of integrated circuit which will powerfully promote the development of China's information industry and play an important role on the development of national economy.

As the integration level is improved, there are more and more crystal valve inside chip and the design is more complex and the technology of computer aided design becomes more important which is a automation design process of electronic products with computer, keeping software as development environment, Hardware Description Language(HDL) as design language, programmable device as experimental carrier. And the tool of design is more important in the design of electronic system. At present, the popular tools of design have divided into three kinds: the first one is professional software company, and the top three are Cadence, Synopsys and Mentor Graphics; the second is one developed by the manufacturer of programmable logic device for selling its products, and the famous ones are Altera, Xilinx and Lattice and so on; the third one is offered by research institutions for academic research, such as the logic synthesis and verification tool ABC[4-5] from University of California, Berkeley. When the FPGA with programmability is used to design, we can freely rewrite its circuit configuration without the paying semiconductor manufacturer development expenses including mask. But the programmability will bring FPGA lower logical density which cost higher with more logic capacity.

On balance, this paper proposed the study of design and application of electronic hardware based on FPGA in which improved the systematic components of traditional FPGA and designed a new FPGA hardware circuit combining the smoothing and Matlab.

2. The Structure and Principle of FPGA

FPGA is a typical re-configurable device and early existed as a semi-custom circuit of ASIC. Now it becomes a new accelerating algorithm part with the help of paralleled algorithms of FPGA. Owing to few resources, early FPGA was only used to realize the simple logic, such as glue logic among the chips, having difficulty to realize the floating point arithmetic. Now FPGA can offer a specialized arithmetic module, a lot of logical resource and storage resource as well as external memory interface, network interface, and other peripheral interfaces which supplies conditions for establishing high performance computing.

FPGA is mainly composed of 6 parts that are programmable put in-out unit, basic programmable logic unit, embedded RAM, abundant arrangement of wire, bottom embedded function unit, embedded specialized hardware module. The bottom embedded function unit includes DSP, PLL, DLL, digital clock management and embedded processor. And the embedded specialized hardware module refers to the hard core with low universality which is generally used in specific field, such as

SERDES used in high-end communication and Ethernet MAC, etc. shown in the Figure 1.

3. Design Flow of Traditional FPGA

FPGA is a kind of programmable logic device with high integration density coming from Xinlix, an American company which created the first FPGA chip in 1985. During the past two decades, the structure and the software development have been improving. The early 1200 usable gates have developed into several hundred thousand of gates and now ten million of gates. Xihnx and Ahera other top-level manufacturers has improved the integration level of FPGA into a new level. FPGA has combined the micro-electronic technique, circuit technique and EDA technique which helps designer concentrate on the design required logic function and cut down the design cycle and improve the quality. The modern design of FPGA applies the Top-down method whose procedures are: behavior design, structure design, logic design, circuit design and layout design. This procedure is that EDA develop software and programming tools develop the devices and its general design flow is shown in figure 2, including preparation of design, input of design, functional simulation, design treatment, time sequence simulation and programming and testing of device.

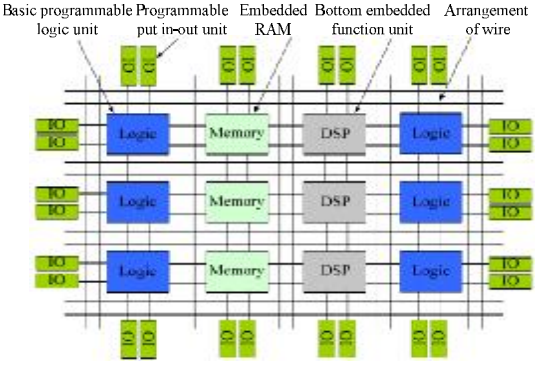

Figure 1. Structural unit inside FPGA

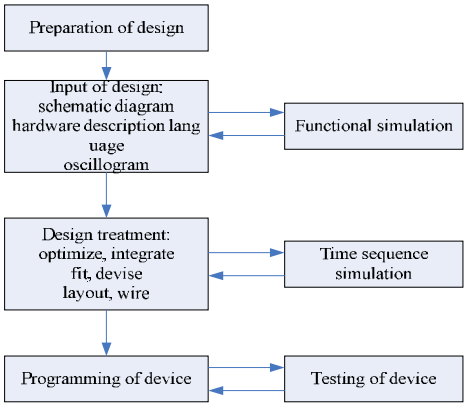

Figure 2. Design flow

4. Design principle of FPGA

4.1. Design principle of filtering base band

The paper adopts the method combined FPGA and Matlab which helps FPGA complete three functions above, and at the beginning stimulates the system and produces the important parameter required in design of VHDL. During the design, the difficult arithmetic that FPGA cannot realize can be transferred to Matlab. In the end, the intermediate results operating on hardware are led into Matlab. Through the drawing oscillogram and eye pattern, each design can be checked. Matlab simulation will be integrated into the design of FPGA which resolves the difficulties in FPGA debugging and frequently inconsistent conditions with the system simulation logic.

4.2. The simulation testing of FPGA filter

During the using and testing of Matlab, firstly the shaped single y (n) will be sequence simulated after receiving filter Gr (O in the Medelsim. And then output the z (n), the convolution results at every moment and save in a txt document. Matlab read all the data of z(n) and calculate and draw the oscillogram and eye pattern shown in Figure 3, 4. The Figure 3 and 4 are respectively the oscillogram and the eye pattern in which the filter's roll-off factor a=1, the superposition of variance of white gaussian noise in the channel is 0.3456, after receiving filter Gr(O y(n) receives the signal z(n).

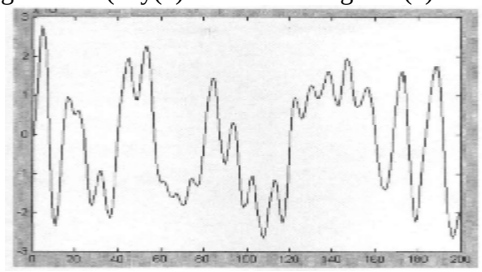

Figure 3. The oscillogram of z(n) when the superposition of variance of white gaussian noise is 0.3456

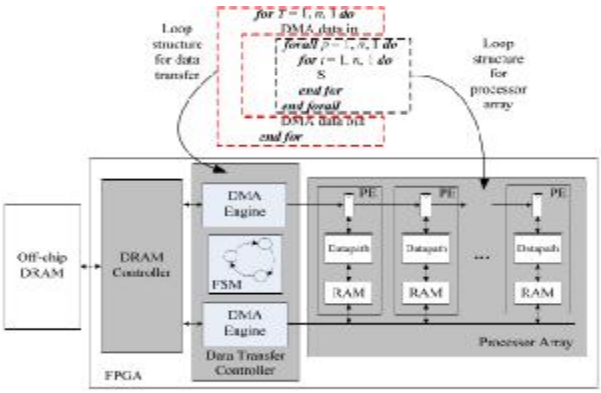

Figure 4. The eye pattern of z(n) when the superposition of variance of white gaussian noise is 0.3456

In Figure 4, we can find that the range of eye is wider and the system can tolerate the noise in a wide range. When receiving the decision, the best decision threshold is zero, and the systematical error rate is in the normal limits and can effectively filter the high-frequency component.

This design adopts "m" as the information source of systematical input, and meanwhile, the single polarity element will be transferred into the bipolar element. When using the PFGA, it applies cascade of four D-flip flop to produce a "m" sequence with 15(24-l) perimeter. And the lbit will be expanded into Zbit, which +l is coded into 01,-l is coded into 11 and the first one is sign bit. And in one clock period, the Zbit will be transmitted that means the rate of code element will be doubled. When information source produces module, the time sequence simulation is shown in Figure 5 in which din is the original single polar code and dmod is the bipolar code after coding.

After confirming the distribution of data, the scheduling mode will be decided. According to the distribution of block cyclic data, each FPGA block distribute the iteration block visiting the data of local DRAM. As shown in Figure 5, being same as the data transmission management of mono-block FPGA, there are two scheduling plans of the multi-block FPGA iteration block: scheduling plan one and scheduling plan two, the number in the Figure 5 implies the sequence. The data in the external memory is stored in line. With the same reason that the data transmission mechanism two of mono-block FPGA is superior to the data transmission mechanism one, scheduling plan two of multi-block FPGA is superior to scheduling plan one.

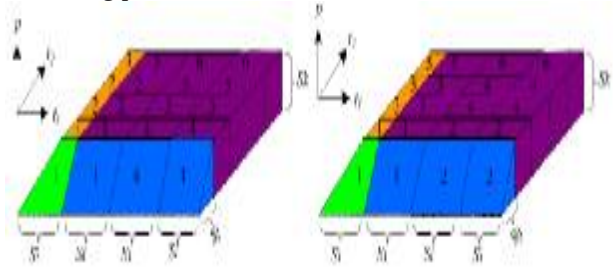

Figure 5. Scheduling plan of multi-block FPGA

The Figure 6 is a time sequence simulation in which dout--gen is single polar code input by system; dout--result is the signal after receiving the decision; dout--total is the total code element; dout-rong is the wrong code element. Through the filtering, noise addition and receiving decision, the input signal is delayed several clock than the source. When counting the wrong code element, the first right code element should match the source unless the performance cannot be analyzed correctly.

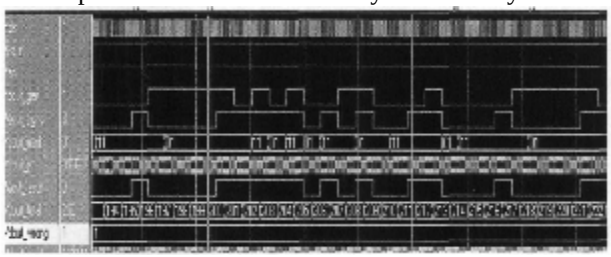

Figure 6 System simulation of FPGA

5. Conclusion

The paper based on the traditional FPGA and gave a design and application of hardware combined FPGA and Matlab. The results of the simulation and testing of the signal in the FPGA noise shows that this design, compared with the traditional FPGA, has less error and stronger ability of denoising and has more value in theory. The system gives the better performance and meets the requirement of the design.

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