Research on the Packaging Technology for Integrated Power Electronics Module

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Abstract: Power electronic system integration is a comprehensive project of cross-infiltration of power electronics technology and materials, machinery, chemistry, information and other multi-disciplinary edges. It can realize high power density, high efficiency, high reliability and low cost of power electronic systems and is the important direction of the development of power electronics technology. This paper mainly introduces the key technologies of integrated power electronic module packaging such as membrane technology, substrate technology, package structure and interconnection technology. Based on this, this paper uses flip chip technology to complete the design and packaging of half-bridge FC-IPEM. Finally, the electrical performance of FC-IPEM is tested briefly to provide some guidance for the integration of power electronic systems.

Keywords: Power electronics system integration; Integrated Power electronics module (IPEM); Modeling; Three-dimensional packaging; Flip chip technology (FCT)

1. Introduction

Power electronics system integration is a hybrid and complex work, Which involves several subjects such as material, mechanics, chemistry, informatics and so on. It can realize high power density, high efficiency, high reliability and low cost for power electronics system, and it is an important development orientation of power electronics technology. The package technology, which impacts on electrical, EMI and thermal characteristic of the module, is an important part of power electronics system integration. Packaging is considered as a central driver in future power electronics technology. In power electronics integrated system, the discrete parts are replaced by Integrated Power Electronics Modules (IPEMs). This dissertation will focus on the package technology of IPEM.

2. Overview of Power Electronics Integration System

The idea of power electronic system integration is to use the method of integrated system to combine the intelligent universal power electronic standard module together like building blocks, and to form various power conversion systems conveniently. In the power electronic integration system, the discrete components are replaced by the standardized module, IPEM. Taking Distributed Power Sytem as an example, the Power electronic system integration is divided into three levels:

System. It refers to a specific power conversion system, such as a distributed power supply system.

Power electronics standard module. It refers to the subsystem that constitutes the system, such as AC/DC module, DC/AC module, DC/DC module. Power electronic standard module is required to have standard power, heat treatment capacity and control interface, which can not only complete a certain power conversion independently, but also can be combined into large system flexibly and flexibly.

Switch unit and element unit, which constitute the basic unit of power electronics standard module, such as switch bridge arm and filter (filter inductance and filter capacitance) in DC/DC module.

Research and development of power electronic integration system aims to: to the microprocessor (DSP and/or CPU) as the core, such as the required modules like blocks easily combined together, form a organic whole, through the change of software, the flexibility to achieve a variety of different control strategies, to meet the requirements of different systems of the practical work. In the existing research and development, the above ideas are reflected in different degrees, but they do not start from the height of adapting to different systems, so the modules developed are poor in universality and flexibility.

3. Key Technology of Integrated Power Electronic Module Package

3.1. Membrane technology

After power electronic devices entered the transistor era, membrane technology became one of the core technologies of electronic packaging. The thickness of the film is very small, which can be regarded as the twodimensional form of matter. Membrane is divided into thin film and thick film, but there is no strict limit beInternational Journal of Intelligent Information and Management Science ISSN: 2307-0692, Volume 7, Issue 5, October, 2018

tween thin film and thick film. It is generally believed that the film can only be formed on the substrate, and the composition of the film is deposited by vacuum method and solution method. Thick film can be formed independently without matrix. It is formed by slurry printing. A film with thickness greater than 1 micrometer is called thick film.

3.2. Substrate technology

The substrate provides effective interconnection between chips and components and mechanical support of modules, which is the foundation of modules. When selecting substrate materials, consider the following properties:

Mechanical performance: high enough mechanical strength as the mechanical support of the module; Easy to process, high dimensional accuracy; The surface is bright and clean, smooth and without micro cracks.

Electrical performance: high insulation performance; Low dielectric constant; Small dielectric loss; The performance is stable under the condition of high temperature and high humidity.

Thermal performance: high thermal conductivity; Good heat resistance; CTE is matched with related materials. Other properties: good chemical stability; No hygroscopic property; Easy to manufacture and low cost. The dielectric constant, CTE and thermal conductivity of the substrate material have important effects on the performance of the substrate. There are many materials used to make the substrate. According to the basic materials of the substrate, the substrate can be divided into organic class, inorganic class and composite class. In power electronics module packaging, DBC ceramic substrate, insulating metal substrate, glass cloth substrate, flexible substrate, etc.

Flexible Printed Circuit Board (Flexible Printed Circuit Board) is a Printed Circuit Board made by pressing Flexible insulating substrate, copper foil and covering film with both mechanical protection and good electrical insulation performance. The substrate is mainly polyimide, as shown in figure 1. Flexible printed circuit board has high heat resistance and good dimensional stability. It can be freely bent, wound and folded. It can move and expand in 3d space according to the requirements of spatial layout, so as to achieve the integration of component assembly and wire connection. The surface and inner conductor of double-sided and multi-layer printed circuit board can realize the electrical connection of inner and outer circuit through metallization.

3.3. Encapsulation structure and interconnection technology

Generally, the packaging of power devices and power modules is based on thin film thick film technology, welding technology, mechanical connection and so on. Here is the introduction of welding technology. Welding refers to the process of combining atoms to form a permanent connection between materials (of the same material or of a different material) by heating, pressing, or

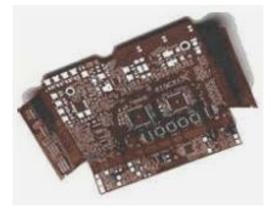


Figure 1. Flexible substrate

both. According to the characteristics of welding process, it can be divided into melting welding, pressure welding and brazing. Brazing is the first interconnection method, which USES metal materials lower than the melting point of the base metal as solder, heats the solder and solder, makes the solder melt but the solder does not melt. With the miniaturization of the interconnection position, brazing becomes difficult, so pressure welding is adopted. Common pressure welding methods include hot pressure welding and ultrasonic welding.

4. Design and packaging of FC-IPEM

4.1. Design of FC-IPEM

The circuit diagram of half-bridge IPEM is shown in figure 2. Q1 and Q2 are two MOSFET, which contain a reverse diode. The HIP2100 is a 100V half-bridge N channel MOSFET drive chip consisting of input logic circuits, level converters, high-end power transistor drive levels and low-end power transistor drive levels. C2 is the filter capacitor of the working power supply of the chip. C3 and a diode inside the chip constitute a lifting power supply mode. The 5 feet and 6 feet of the chip are the input terminals of the high side and low side MOS-FET control signals, and 3 feet and 8 feet are the output terminals of the high side and low side MOSFET drive signals, providing drive signals for Q1 and Q2 respectively. R1~R4 are drive circuit resistance of Q1 and Q2 respectively. The half-bridge IPEM has three large current terminals, P and N are the positive and negative terminals of the input dc power supply respectively, and O is the middle lead terminal. C1 is the power bus filter capacitance.



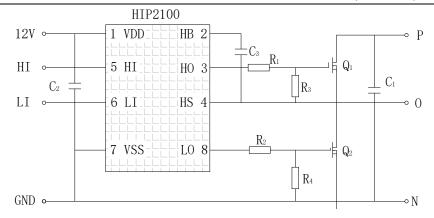


Figure 2. Circuit schematic diagram of half-bridge FC-IPEM

The three-dimensional packaging structure of FC-IPEM is shown in figure 3. The power chip is sandwiched between a high thermal conductivity substrate (bottom) and a double-sided PCB (top). By using the flip chip technology, the source area of the chip is connected with the corresponding pad on the PCB underside through the solder bump. The back of the chip is welded to the underlying substrate. In this way, the heat generated in the chip can be directly dissipated through the underlying substrate at the back of the chip and transmitted to the PCB through the welding spot. To match the CTE of the solder joint, the substrate material, and the chip, a gap is filled around the solder joint and between the chip and the substrate.

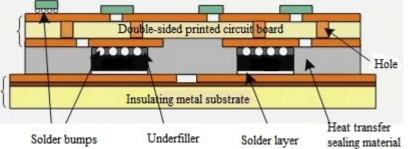


Figure 3. FC-IPEM structure diagram

The thermal conductive sealing material is filled between the PCB and the bottom substrate to realize 3d heat dissipation. Finally, by using surface assembly technology or flip chip technology, drive, protection and other circuit devices are welded to the top layer of PCB. In fc-ipem, solder convex points are used to connect with the top substrate, which completely cancels the bonding process of leads, and the interconnection distance is small, effectively reducing parasitic parameters. Three-dimensional packaging structure, increased heat transfer path, more easy to heat. The device is sealed and the package is more reliable.

4.2. Fc-ipem packaging

The specific packaging procedure of half-bridge FC-IPEM is as follows:

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On the workbench PRC2000E hot repair heating plate, using high temperature solder (Sn95 / Ag5, solid, melting point 221 $^{\circ}$ C) on the aluminum base plate welding large current copper terminal.

In FR - 4 base slabs should be MOSFET welding plate position, coating temperature solder (Sn63 / Pb37, paste, melting point 183 °C), heat melt after cooling. On the mp-2000 micro optical alignment system, the power chip solder bump point and the top layer PCB welding pad are aligned, and then the welding is performed through the Electrovert omniflo7 hot air reflux welding furnace with 7 heating zones. All welding is completed at the same time. The temperature setting of reflow furnace is shown in table 1, and the belt speed is 0.5m/min.

Table 1.	Temperature	Settings	for reflow	furnace
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Temperature range	1	2	3	4	5	6	7
Top temperature	100	120	130	140	165	235	190
Bottom temperature	100	120	130	140	165	235	190

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The flip chip soldered chip is cleaned, and the underfill material is filled in the gap around the solder joint and between the chip and the FR-4 substrate. During operation, the two edges of the chip are filled in an "L" shape, which is carried out on the heating plate. So far, the device is secure and reliable for operation.

Using a low-temperature solder (Sn 43/ Pb 43 /Bi 14, paste, melting point 163 $^{\circ}$ C), the chip-bonded FR-4 substrate and the aluminum substrate are butt welded, and a heat conduction seal is filled between the FR-4 substrate and the aluminum substrate. material.

Using surface mount technology, the use of low temperature solder (Sn43 / Bi57, paste, melting point is 135 $^{\circ}$ C), the FR - 4 substrate welding drive and protection circuit devices. Fc-ipem is successfully packaged with a base plate size of 50 x 50 mm, as shown in figure 4.

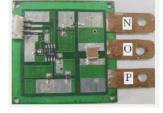


Figure 4. Half-bridge FC-IPEM

5. Electrical Performance Testing of FC-IPEM

In order to test the electrical performance of the halfbridge fc-ipem, the synchronous rectifier Buck converter is constructed by using it. The circuit schematic diagram is shown in figure 5. The P and N terminals of the halfbridge fc-ipem are connected to the input voltage Vin and O terminals are connected to the filter inductor Lf. The data used in the experiment were: the input voltage Vin=42V, the output voltage Vo=12V, the output current Io=3A, and the operating frequency fs=105kHz. When designing Lf, the maximum ripple of output filtered inductance current is 20% of Io. FIG. 6 shows the experimental waveform when the output is fully loaded, and presents the drain-source voltage waveforms vDS(Q1) and vDS(Q2) of Q1 and Q2, as well as the current waveform iLf in the output filter inductance. It can be seen that the half-bridge FC-IPEM synchronous rectifier Buck converter works normally. The small leakage peak voltage of Q1 and Q2 indicates that the structure of fc-ipem effectively reduces parasitic inductance.

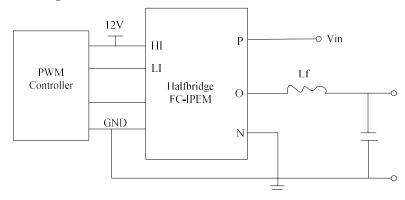


Figure 5. Half-bridge FC-IPEM synchronous rectifier buck converter

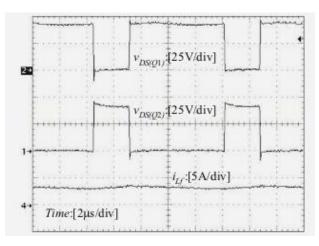


Figure 6. Experimental waveform

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6. Conclusion

Power electronic system integration is a comprehensive project of power electronic technology intercrossing with materials, machinery, chemistry, information and so on, which is an important direction of power electronic technology development. In the 21st century, with the rapid development of high and new technology, the competition in the international power electronics market is more intense. The creative and high starting point of power electronic system integration research and development can improve the level of power electronic technology development in China, and promote the revolutionary transformation of China's information, energy, materials, industrial production process automation and other related industries.

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